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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,487	08/30/2001	Eugene H. Cloud	4296.1US (00-0054.1)	2698
24247	7590	07/20/2004	EXAMINER FARAHANI, DANA	
TRASK BRITT P.O. BOX 2550 SALT LAKE CITY, UT 84110			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 07/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

09/944,487

Applicant(s)

CLOUD ET AL.

Examiner

Dana Farahani

Art Unit

2814

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 25 June 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
- ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) ☐ they raise the issue of new matter (see Note below);
 - (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____

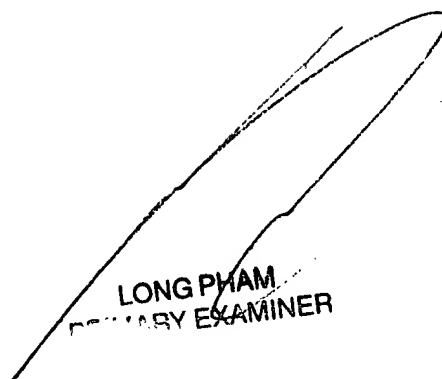
Claim(s) objected to: _____

Claim(s) rejected: _____

Claim(s) withdrawn from consideration: _____

8. ☐ The drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
10. ☐ Other: _____

Continuation of 5. does NOT place the application in condition for allowance because: the Hultmark et al. reference discloses in figures 2A and 2B, the first die 26 and the second die 30 being oriented toward each other.


LONG PHAM
PRIMARY EXAMINER

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-7, 9-16, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hultmark et al., hereinafter Hultmark (U.S. Patent 6,232,667), previously cited, in view of Cobbley et al., hereinafter Cobbley (U.S. Patent 6,064,120), also previously cited.

Regarding claims 1, 7, and 42, Hultmark discloses in figures 2A and 2B, a method for interconnecting at least two semiconductor dice, 26 and 30, comprising: providing a first semiconductor die 26, including a plurality of bond pads 31, arranged in an array over an active surface thereof; providing at least one second semiconductor die 30 including a plurality of bond pads 29 on an active surface thereof; and orienting said first semiconductor die and said at least one second semiconductor die with said active surfaces thereof facing each other such that some bond pads of die 26 remain exposed and some bond pads of die 26 are electrically connected with the corresponding pads of die 30.

Hultmark does not disclose recessed bond pads.

Cobbley discloses in figure 5, recessed bond pads 34, which are included in the structure in order to bring the pads to appropriate contacts with electrodes 20 (see

Art Unit: 2814

column 2, lines 30-43). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use recessed bond pads in Hultmark structure to facilitate bonding procedure between the bond pads and other bond pads and electrodes which will be connected to the recessed bond pads.

Regarding claims 2 and 3, see Hultmark, column 5, line 21, wherein it is stated that the chips may be memory devices and logic dice

Regarding claims 4-6, in Hultmark, conductive solder bumps 32 are directly between pads of the semiconductor dice 26 and 30.

Regarding claim 9-11, in figure 1 of Hultmark a carrier 20, with recess 21, is provided with contacts 33 on a surface thereof, and the first die is oriented such that pads 33 are connected with the corresponding pads of die 26.

Regarding claims 12 and 41, in Hultmark, the second die is in the recess, and a cover sealing 35 is over the two dies.

Regarding claim 13, in Hultmark, leads 33 correspond to the exposed pads of the first die.

Regarding claims 14-16, in Hultmark, conductive solder bumps elements 32 are between the bond pads of the substrate and the first die.

3. Claims 17, 18, 20-24, 26-34, and 36-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hultmark in view of Cobbley, as applied to claim 1 above, and further in view of Buckley, III et al., hereinafter Buckley (U.S. Patent 5,477,082), previously cited.

Art Unit: 2814

Regarding claims 17, 18, 20-22, 33, 34, and 36-38, Hultmark in view of Cobbley renders obvious the limitations in the claims, as discussed above, except for the conductive element having first and second members.

Buckley discloses in figure 4 conductive elements 66 and 72, secured to each other, between chips 58 and 56. Also, shown in the figure, is a third conductive member (secured to the other two), element 76, between the two dice. This arrangement increases heat transfer between the two chips (see column 3, line 52). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use such an arrangement in order to increase the heat transfer between the two chips in Hultmark structure.

Regarding claims 23 and 24, Hultmark discloses the limitations in the claims, as discussed above in regard to claim 1, except for the first and second semiconductor dice are connected to each other via laterally discrete, physically unconnected conductive structures.

Buckley discloses in figure 4, the two dice 56 and 58 are connected to each other via laterally discrete, physically unconnected conductive structures 66 and 72. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use such an arrangement in order to reduce the conductive path between the two dice and increase the heat transfer between the two in Hultmark structure.

Regarding claims 26-28, in figure 1 of Hultmark encapsulant 35 is deposited over at least the first die and between the carrier and the first die, and covers the first die (see column 5, lines 61-63).

Art Unit: 2814

Regarding claim 29, in figure 1 of Hultmark, pads 33 are on the surface of the substrate.

Regarding claim 30, in figure 1 of Hultmark, there is a recess 21 in the surface of the substrate.

Regarding claim 31, in figure 1 of Hultmark, the second die is disposed in the recess of the substrate.

Regarding claim 32, in figure 1 of Hultmark, leads 33 of the substrate correspond to the bond pads of the first die, which are exposed to the periphery of die 2.

4. Claims 19 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hultmark in view of Cobbley and Buckley, as applied to claims 34 and 18 above, and further in view of Baba (U.S. Patent 6,317,333), previously cited.

Hultmark in view of Cobbley and Buckley renders obvious the limitations in the claims, as discussed above, except for the members of the conductive elements being secured directly to each other.

Baba discloses in figure 3a conductive elements 5a and 5b, of chips 2 and 1, respectively, are directly connected as shown in figure 3b. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to secure the conductive elements of the Buckley structure directly to each other in order to take advantage of the property of direct heat transfer between the two conductive elements.

5. Claims 39, 40, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hultmark in view Cobbley and further in view of Yu et al., hereinafter Yu (U.S. Patent 6,100,593), previously cited.

Art Unit: 2814

Hultmark in view of Cobbley renders obvious the claimed invention, as discussed above in regard to claim 1, except for a multi-chip configuration.

Yu teaches in figure 3, a multi-chip configuration that improves the performance of the device in which the chips are used therein, and improves the yield (see paragraph 2, lines 20-24). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use a multi-chip configuration in Hultmark structure, as Yu teaches, since it is well known in the art that using a multi-chip configuration improves the characteristics of the devices that the chips are used in.

Response to Arguments

6. Applicants' arguments filed on 11/14/03 have been fully considered but they are not persuasive.

Applicants argue that the newly added limitation, namely, "...by aligning a peripheral edge of the at least one second semiconductor die with an alignment structure disposed on the active surface of the first semiconductor die" is not in the cited references. However, note that the Hultmark reference shows in figures 2A and 2B, the first die 26 has in fact an alignment structure (31 and 32) on its active surface. Moreover, the second die 30 has a peripheral edge, which is aligned with the alignment structure that consist of elements 31 and 32.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (571)272-1706. The examiner can normally be reached on M-F 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571)272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

D. Farahani

Wael Farahani
SPE 2814